

Serial No.: 10/583,844

PF030184

Remarks

In view of the above amendments to the claims and following discussion, the applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U. S. C. § 102, or obvious under the provisions of 35 U. S. C. § 103. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

A. 35 U. S. C. § 102

1. Claims 1-5, 8, 11 and 13 are patentable over Koyama et al.

Claims 1-5, 8, 11 and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003). The applicants submit that these claims are not anticipated in this reference.

The present invention relates to a display screen comprising light emitters arranged in rows and columns to form an array of light emitters, which are fabricated on a silicon substrate, in particular on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate by using a pulsed excimer laser. The light emitters are controlled by modulation transistors, which are in particular thin film transistors produced on the polycrystalline silicon substrate. However, thin film transistors of this kind have dispersions of the threshold trigger voltage and non-uniformities in the levels of current flowing through them for a given voltage applied to their gates. This results in variations of luminance of the light emitters. To compensate for these dispersions, it is known to use compensating transistors for compensating the variations of the threshold trigger voltages, see Applicant's specification at page 1, lines 16 – 34.

Serial No.: 10/583,844

PF030184

The object of the present invention is to provide a display screen of this kind which uses one compensating transistor for each column, for compensating the threshold trigger voltages of all modulation transistors within a column by only one compensating transistor, which display screen has a uniform luminance of all of the light emitters.

This object is solved according to the new claim 1 by aligning all modulation transistors of a column associated with the column of light emitters on a substrate according to a guiding line, and providing a single compensating transistor connected to all the modulation transistors of a given column, wherein:

the modulation transistors are arranged in columns associated with the columns of light emitters and are geometrically aligned on the substrate along a guiding line,

each compensating transistor of a given column is formed in the geometrical extension of the line-arrangement of the modulation transistors of said given column along the same guiding line,

the modulation transistors and the associated compensating transistor are fabricated on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate, using a laser beam, said beam being intended first to heat a first rectangular heating surface of the substrate, then to move in a direction of movement and then to heat a second rectangular heating surface, and

the modulation transistors associated with the light emitters of a given column and the associated compensating transistor are aligned in one and the same rectangular heating surface, the guiding alignment line extending approximately perpendicularly to the direction of movement of the laser beam.

Because the modulation transistors and the respective compensating transistor have been fabricated on the same rectangular heating surface, they have similar threshold trigger voltages and therefore, the drain current flowing through the modulation transistors is independent of its threshold trigger voltage, as explained on pages 13 - 15 in the description of the present invention.

Serial No.: 10/583,844

PF030184

The reference Koyama, US 2003/0107534, describes an active matrix display screen comprising light emitters arranged in rows and columns to form an array of light emitters, which are fabricated for example on a polycrystalline silicon substrate. The light emitters are controlled by modulation transistors, in particular thin film transistors produced on the polycrystalline silicon substrate, see Koyama at paragraph 0199.

To compensate for the variation of the threshold trigger voltages of the modulation transistors and to provide a current to the light emitters corresponding linearly to a video signal, Koyama teaches to couple a correction transistor in parallel to an operation amplifier, which is arranged as a line driver for all the modulation transistors of a given column, see Koyama at Figs. 1, 6, 9. An inputted analog video signal is converted into a current, i.e. by using a resistor in front of the operation amplifier, see Koyama at paragraph 0083. This current is converted by the operation amplifier into the gate-source voltage of the correction transistor, which correction transistor has the same polarity as the modulation transistors, to which the gate-source voltage is supplied via a source signal line coupled to a gate electrode of the modulation transistors. Thus, the light emitters of a corresponding column can emit light at a luminance, which corresponds linearly to the inputted analog signal voltage, see Abstract of Koyama and the embodiments.

The reference Koyama therefore uses a compensation method for the display screen, which is essentially different from the compensation arrangement as described by the new claim 1 of the present invention:

provide a compensating transistor of a given column in the geometrical extension of the line-arrangement of the said modulation transistors of said given column,

use a laser beam for heating a first rectangular heating surface of the substrate, then to move in a

Serial No.: 10/583,844

PF030184

direction of movement and then to heat a second rectangular heating surface, and

arrange the compensating transistor together with the corresponding modulation transistors within such a rectangular heating surface for heating the compensating transistor together with the corresponding modulation transistors for the same time.

The reference Hatano, US 2004/0017365, describes an active matrix display screen comprising light emitters arranged in rows and columns to form an array of light emitters, which are fabricated for example on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate by using a laser. The light emitters are controlled by modulation transistors, in particular thin film transistors produced on the polycrystalline silicon substrate. By providing a display screen of this kind, there is a limit to the carrier mobility in a channel between a source electrode and a drain electrode of the thin film transistors, which is related to a grain boundary of each of the crystal grains of the polycrystalline silicon film crystallized by irradiation of the laser light, see Hatano at paragraph 0011.

To overcome this problem, Hatano uses selectively enlarging laser crystallization (SELAX), as described in paragraphs 0013, 0014, to obtain a crystallized silicon film which has its longitudinal direction arranged with the scanning direction of the laser light, paragraph 0022. This laser crystallization method provides silicon films with grain boundaries in generally one direction, which grain boundaries correspond with the direction of movements of the carriers of the thin film transistors, see Abstract and claim 1. Therefore, the carrier mobility is increased in the channel of the thin film transistors.

Serial No.: 10/583,844

PF030184

The reference Hatano therefore is not related to the problem, how to compensate the threshold trigger voltage of thin film transistors. Correspondingly, Hatano does not give a person skilled in the art any hints into this direction.

Hatano in particular does not disclose to heat a first rectangular heating surface, in which a compensating transistor is included together with the corresponding modulation transistors of a column, then move in a direction of movement and then to heat a second rectangular heating surface including a compensating transistor together with the corresponding modulation transistors.

Hatano in particular does not teach to use a stepwise heating of rectangular surfaces including a compensating transistor together with the corresponding modulation transistors, or gives any hints into this direction, because Hatano uses a laser beam to form discontinuous converted regions of roughly band shaped crystal silicon films having grain boundaries continuous in generally in one direction, see claim 1 of Hatano. Hatano therefore teaches heating of a silicon substrate, which is completely different from the heating, as disclosed in the new claim 1.

The problem described and solved by Hatano is also essentially different from the problem as described by Koyama, and is in particular not related to the problem to compensate for the variation of the threshold trigger voltages. A person skilled in the art therefore does not see any motivation, to apply the method of heating of a silicon substrate as described by Hatano to a display device as described by Koyama.

Even, if a person skilled in the art would apply the teaching of Hatano to a display screen as described by Koyama, he would not arrive at a display screen as defined in the new claim 1, because Hatano does not teach to heat a first rectangular heating surface, in which a compensating transistor is included together with the corresponding modulation transistors of a column, then move in a direction of movement and then to heat a second rectangular heating surface including a compensating transistor together with the corresponding modulation transistors.

Serial No.: 10/583,844

PF030184

In particular, no prior art teaches to use such a heating method which uses a stepwise heating of rectangular surfaces including a compensating transistor together with the corresponding modulation transistors as described in the new claim 1, or gives any hints into this direction. The new claim 1 is therefore new and inventive over the cited references.

Consequently, as claim 1 is not described in Koyama et al. and/or Hatano, claim 1 is patentable thereover.

Claims 2-5, 8, 11 and 13 depend directly from claim 1. In view of the above arguments, claims 2-5, 8, 11 and 13 are also patentable over Koyama et al. and/or Hatano based on their dependence on claim 1.

B. 35 U. S. C. § 103

1. Claims 7 and 12 are patentable over Koyama et al.

Claims 7 and 12 stand rejected under 35 U.S.C.103(a) as being unpatentable over Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003). The applicants submit that these claims are not rendered obvious by this reference.

Claim 7 recites that, in the display screen as claimed in claim 1, the said modulation transistors and the said associated compensating transistor each include a channel between two layers of doped material, the said channel being connected to their gate electrode, and in that the channel of the modulation transistors of a column and the channel of the associated compensating transistor have a main axis approximately parallel to the said guiding line 72. At page 13, lines 26-31 of applicant's specification, it is stated that "the modulation transistors 14, 24 and 34 and the compensating transistor 48 are produced such that their drain channel has a main axis approximately perpendicular to the direction 68 of movement of the laser beam", i.e. parallel to the said guiding line 72. Using such an orientation of the channel parallel to the

Serial No.: 10/583,844

PF030184

guiding line 72 make it easier to insert the transistors on the rectangular surfaces 66 heated by the laser beam, because these heated rectangular surfaces 66 are narrow and may be narrower than the length of the channels to fabricate. Therefore, using such a orientation of the channel parallel to the guiding line 72 enhance still further the similarities of the threshold trigger voltage V_{th14} , ... of the modulation transistors with the threshold trigger voltage V_{th48} of the compensating transistors 48 of the same column, then providing a further enhancement of the compensation of the threshold trigger voltage V_{th14} , ... as stated in applicant's specification at page 13, lines 33-37.

With regard to claim 7, the Examiner admits that "Koyama et al. does not disclose the main axis is parallel to the guiding line". But the Examiner considers that, "At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to change the orientation of the transistors (i.e. channels) because applicants have not disclosed that the specific orientation as claimed provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a different transistor orientation because it would not have a significant, if any, impact of the performance of the circuit." The applicants strongly disagree with this statement, on the grounds developed in the previous paragraph showing the advantages of the claimed orientation.

Consequently, claims 7 and 12 which depend from claim 1 are patentable over Koyama et al.

3. Claims 9-10 are patentable over Koyama et al. in view of Lo

Claims 9-10 stand rejected under 35 U.S.C.103(a) as being unpatentable over Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003) in view of Lo (U. S. Patent 6,937,215 issued August 30, 2005). The

Serial No.: 10/583,844

PF030184

applicants submit that these claims are not rendered obvious by the combination of these references.

Claim 9 recites that, in the display screen as claimed in claim 1, wherein the control means (2, 10, 20, 30, 40, 42, 44, 46, 48, 50) include initialization means (50) for initializing the load capacitors (16, 26, 36) intended to discharge all the load capacitors connected to the modulation transistors of a column (claim 8), the initialization means (50) include an initialization transistor (50) having a gate electrode and two current-carrying electrodes, one current-carrying electrode of the said initialization transistor (50) being connected to the gate electrode of the modulation transistors (14, 24, 34) of the said column, the gate electrode of the said initialization transistor (50) being connected to a current-carrying electrode and to the addressing electrode (40) of a column of light emitters.

The Examiner indicated that Koyama et al. discloses everything claimed as applied above (see claim 8), in addition, Koyama et al. discloses wherein the initialization means include an initialization transistor having a gate electrode and two current-carrying electrodes, one current-carrying electrode of the said initialization transistor being connected to the gate electrode of the modulation transistors of the said column [reset TFT 117, figure 11], however, Koyama et al. fails to disclose "the gate electrode of the said initialization transistor being connected to a current-carrying electrode and to the addressing electrode of a column of light emitters".

In Lo, the gate electrode G of the initialization transistor T4 (FIGS. 1-3) is indeed connected to a current-carrying electrode D of this transistor, and to an electrode 111. However, instead of being an "addressing electrode of a column of light emitters" as recited in claim 9, this electrode 111 is a so-called "previous scan line », which is definitely NOT an "addressing electrode" but a "scan electrode".

Therefore, Lo cannot teach the claimed invention, and claim 9 which depends on claim 1 is patentable over Koyama et al. in view of Lo.

Serial No.: 10/583,844

FF030184

Claim 10 recites that, in the display screen as claimed in claim 1, wherein the control means (2, 10, 20, 30, 40, 42, 44, 46, 48, 50) include initialization means (50) for initializing the load capacitors (16, 26, 36) intended to discharge all the load capacitors connected to the modulation transistors of a column (claim 8), the initialization means (50) include a diode, the cathode of which is connected to the gate electrode of the modulation transistors (14, 24, 34) and the anode of which is connected to the addressing electrode (40) of a column of light emitters.

In Lo, as the gate electrode G of the initialization transistor T4 (FIGS. 1-3) is connected to a current-carrying electrode D of this transistor, this initialization transistor T4 works indeed as a diode. But the current-carrying electrode D is connected an electrode 111, which is definitely NOT an "addressing electrode" but a "scan electrode" (see above).

Therefore, Lo cannot teach the claimed invention, and claim 10 which depends on claim 1 is patentable over Koyama et al. in view of Lo.

CONCLUSION

Thus, the applicants submit that none of the claims, presently in the application, are anticipated under the provisions of 35 U. S. C. § 102, or obvious under the provisions of 35 U. S. C. § 103. Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

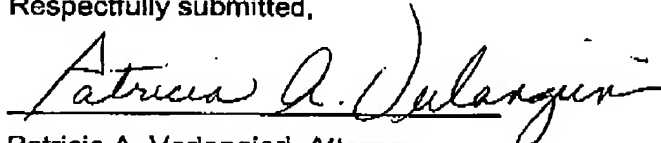
If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application,

Serial No.: 10/583,844

PF030184

it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867, so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



Patricia A. Verlangieri, Attorney
Reg. No. 42,201
(609) 734-6867

Patent Operations
Thomson Licensing LLC.
P. O. Box 5312
Princeton, New Jersey 08543-5312

February 28, 2010